中文摘要

本論文提出創新的採用統計型時間數位轉換器的全數位頻率合成器，統計型時間數位轉換器由全數位的方式實現，透過數學的統計運算能突破製程提供的最小時間解析度—單一個反相器的時間延遲，並免去類比架構設計上達到高解析度需要的複雜匹配。並且若不考慮面積和功耗的情況下，根據數學模型推論可以依要求幾乎無限制的提高時間解析度直到應用所需要的量級。

全數位頻率合成器採用了本論文提出的統計型時間數位轉換器、以及動態改變濾波係數的迴路濾波器、和加速鎖定的鎖定狀態控制電路。設計頻道為 ISM 的 2.4 億赫茲頻帶的 14 個頻道，模擬結果各頻道的鎖定時間均在 8 微秒之內，而鎖定狀態下的頻率誤差都在 1 百萬分之一之內。

關鍵字：統計型時間數位轉換器、全數位頻率合成器、動態迴路濾波器、快速鎖定

ABSTRACT

This thesis proposed an all-digital frequency synthesizer with a novel statistic TDC. The statistic TDC exploits the statistic properties of a set of counters and toggle logics to achieve high resolution - smaller than one minimum inverter delay. The statistic TDC is fully synthesizable and intrinsic have the basic ability to against the process variation from its mathematic model and statistic architecture. In addition, without considering area and power, the statistic TDC can achieve almost unlimited resolution base on the derived mathematical model.

The all-digital frequency synthesizer builds a loop filter which changing coefficient dynamically and a locking stage controller to speed up the locking process. The locking time of the simulation results show that settling time of all the channels in ISM 2.4 GHz band are all within 8us, and the frequency error are all smaller than 1ppm.

Index Terms — Statistic TDC、ADPLL、Dynamic Loop Filter、Fast Locking Technique